WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a memory cell array having memory cells arranged in matrix form;

sense amplifiers which amplify a signal read out from the memory cells and which include N channel sense amplifiers each comprising an N channel MOS transistor and P channel sense amplifiers each comprising a P channel MOS transistor;

a first and second drive circuits each including an N channel MOS transistor which drives the N channel sense amplifiers or P channel sense amplifiers, respectively, included in the sense amplifiers, the first and second drive circuits being arranged adjacent to the sense amplifiers; and

a sense amplifier control circuit which supplies a common control signal to both gate electrodes of the N channel MOS transistors included in the first and second drive circuits.

2. A semiconductor integrated circuit according to claim 1, wherein the P channel MOS transistors each constituting the P channel sense amplifier are formed on an N type well area, the N channel MOS transistors each constituting the N channel sense amplifier are formed on a P type well area located adjacent to the N type well area, and the N channel MOS transistors included in the first and second drive circuits are

formed on the P type well area.

3. A semiconductor integrated circuit according to claim 1, further comprising a plurality of first circuit groups each including the sense amplifiers including the N channel sense amplifier and the P channel sense amplifier, and the first driving circuit driving the N channel sense amplifier, the semiconductor integrated circuit further comprising a plurality of second circuit groups including the sense amplifiers and the second driving circuit driving the N channel sense amplifier,

wherein a transistor size ratio of an N channel MOS transistor possessed by the first driving circuit and an N channel MOS transistor possessed by the second driving circuit is set by changing the numbers of first and second circuit groups arranged to change the numbers of first and second driving circuits.

4. A semiconductor integrated circuit comprising:

a memory cell array having memory cells arranged in matrix form in a row and column directions, the memory cell array being connected to a pair of bit lines;

sense amplifiers which amplify a minor signal read out from the memory cell and appearing between the pair of bit lines, the sense amplifiers each including a P channel sense amplifier comprising a P channel MOS transistor, the sense amplifiers being successively

arranged in the column direction;

drive circuits each comprising an N channel MOS transistor which drives the P channel sense amplifiers included in the sense amplifiers, the drive circuits being successively arranged adjacent to the sense amplifiers in the column direction; and

a sense amplifier control circuit which supplies a control signal to a gate electrode of the N channel MOS transistor included in each of the drive circuit.

5. A semiconductor integrated circuit according to claim 4, wherein one of the drive circuits driving the P channel sense amplifiers is arranged for every two of the sense amplifiers successively arranged in the column direction.

6. A semiconductor integrated circuit according to claim 4, wherein the P channel MOS transistors each constituting the P channel sense amplifier are formed on an N type well area, and a well potential of the N type well area is equal to a drain voltage of the N channel MOS transistor included in each of the drive circuits driving the P channel sense amplifiers.

7. A semiconductor integrated circuit according to claim 4, wherein the P channel MOS transistors each constituting the P channel sense amplifier are formed on the N type well area, the N channel MOS transistors each constituting the N channel sense amplifier are formed on a P type well area located

adjacent to the N type well area, and the N channel MOS transistors included in the drive circuits are formed on the P type well area.

8. A semiconductor integrated circuit comprising:

a memory cell array having memory cells arranged in matrix form in a row and column directions, the memory cell array being connected to a pair of bit lines;

sense amplifiers which amplify a minor signal read out from the memory cells and appearing between the pair of bit lines, the sense amplifiers including N channel sense amplifiers each comprising an N channel MOS transistor and P channel sense amplifiers each comprising a P channel MOS transistor, the sense amplifiers being successively arranged in the column direction;

a first and second drive circuits each including an N channel MOS transistor which drives the N channel sense amplifiers or P channel sense amplifiers, respectively, included in the sense amplifiers, the first and second drive circuits being successively arranged adjacent to the sense amplifiers in the column direction; and

a sense amplifier control circuit which supplies a common control signal to both gate electrodes of the N channel MOS transistors included in the first and second drive circuits.

9. A semiconductor integrated circuit according to claim 8, wherein the P channel MOS transistors each constituting the P channel sense amplifier are formed on an N type well area, the N channel MOS transistors each constituting the N channel sense amplifier are formed on a P type well area located adjacent to the N type well area, and the N channel MOS transistors included in the first and second drive circuits are formed on the P type well area.

10. A semiconductor integrated circuit according to claim 8, wherein the N channel MOS transistor included in the first drive circuit driving the N channel sense amplifiers and the N channel MOS transistor included in the second drive circuit driving the P channel sense amplifiers are arranged in line in the column directions.

11. A semiconductor integrated circuit according to claim 10, wherein a gate length of the N channel MOS transistor included in the first drive circuit is equal to a gate length of the N channel MOS transistor included in the second drive circuit.

12. A semiconductor integrated circuit according to claim 10, wherein a threshold voltage of the N channel MOS transistor included in the first drive circuit is equal to a threshold voltage of the N channel MOS transistor included in the second drive circuit.

13. A semiconductor integrated circuit according to claim 8, wherein the first drive circuit driving the N channel sense amplifiers and the second drive circuit driving the P channel sense amplifiers are arranged for every two of the sense amplifiers successively arranged in the column direction.

14. A semiconductor integrated circuit according to claim 10, wherein the N channel MOS transistors included in the first and second drive circuits, respectively, have a common gate electrode extending in the column direction.

15. A semiconductor integrated circuit according to claim 14, wherein source contacts connected to sources of the N channel MOS transistors included in the first and second drive circuits, respectively, are arranged opposite each other relative to the common gate electrode extending in the column direction.

16. A semiconductor integrated circuit according to claim 8, wherein the P channel MOS transistors each constituting the P channel sense amplifier are formed on an N type well area, and a well potential of the N type well area is equal to a drain voltage of the N channel MOS transistor included in the second drive circuit driving the P channel sense amplifiers.

17. A semiconductor integrated circuit according to claim 8, further comprising a plurality of first circuit groups each including the sense amplifiers

including the N channel sense amplifier and the P channel sense amplifier, and the first driving circuit driving the N channel sense amplifier, the semiconductor integrated circuit further comprising a plurality of second circuit groups each including the sense amplifiers and the second driving circuit driving the N channel sense amplifier,

wherein a transistor size ratio of an N channel MOS transistor possessed by the first driving circuit and an N channel MOS transistor possessed by the second driving circuit is set by changing the numbers of first and second circuit groups arranged to change the numbers of first and second driving circuits.

18. A semiconductor integrated circuit according to claim 8, further comprising an equalize transistor that equalizes a source potential at the N channel MOS transistor constituting the N channel sense amplifier with a source potential at the P channel MOS transistor constituting the P channel sense amplifier, and

the equalize transistor is arranged in a column in which the first and second driving circuits are consecutively arranged.